



HAMED DOROSTI

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EDUCATION

) [University of Tehran](#), ECE Department, Tehran, Iran
Ph.D. Computer Engineering (Computer Architecture), 2011-2017.

Supervisor: Dr. S. M. Fakhraie.

Thesis: Adaptive Timing Error Detection and Correction in Ultra-Low-Power Processors in Nanoscale

) [University of Tehran](#), ECE Department, Tehran, Iran
Master of Science, Computer Engineering (Computer Architecture), 2009-2011.

Supervisor: Dr. S. M. Fakhraie.

Thesis: Quantitative Approach to Specifications of Processor Architecture for Wireless Sensor Networks. (20/20)

) [University of Tehran](#), ECE Department, Tehran, Iran
Bachelor of Science, Computer Engineering, 2005-2009.

Supervisor: Dr. S. M. Fakhraie.

Thesis: Study of Fault Tolerant Techniques in Application Level Using SimpleScalar and PacketBench Simulation Environments. (20/20)

RESEARCH INTERESTS

-) Computer Architecture
-) Design Space Exploration & Power Optimization
-) Network Processor Design
-) Embedded System Design
-) VLSI System Design
-) Digital Signal Processing
-) High Performance Computing
-) Variation Aware Design
-) Adaptive Reliability Enhancement by Online Error Detection and Correction
-) Deep Learning and Artificial Intelligence

CONFERENCE PAPERS

- J E. Salehi Mostafa, Dorosti Hamed, Fakhraie Sied Mehdi, "Architecture Level Design Space Exploration of SuperScalar Microarchitecture for Network Applications," DSD2010, Sep. 2010.
- J Firouzi F., Yazdanbakhsh A., Dorosti H. and Fakhraie Sied Mehdi, "Dynamic Soft Error Hardening via Joing Body Biasing and Dynamic Voltage Scaling," DSD2011, Sep. 2011.
- J Faryabi M., Dorosti H., Modarresi M., Fakhraie S. M., "Process Variation-Aware Approximation for Efficient Timing Management of Digital Circuits," EWDTs 2015.

JOURNAL PAPERS

- J Dorosti, Hamed, Teymouri, Ali, Fakhraie, Sied Mehdi, E. Salehi, Mostafa, "Ultralow-Energy Variation-Aware Design: Adder Architecture Study," IEEE Transaction on Very Large Integration (VLSI) Systems, Vol. 24, No. 3, 2016.
- J Nakhaee F., Kamal M., Afzali-Kusha A., Pedram M., Fakhraie S. M., Dorosti H., "Lifetime Improvement by Exploiting Aggressive Voltage Scaling During Runtime of Error-Resilient Applications," Elsevier Integration The VLSI, Vol. 61, 29-38, 2018.
- J B. Soltani Farani, H. Dorosti, M. E. Salehi, S. M. Fakhraie, "Ultra-low-energy DSP processor design for many-core parallel Applications," JECEI, Vol. 8, No. 1, 71-84, 2020.
- J A. Teymouri, H. Dorosti, M. E. Salehi, S. M. Fakhraie, "Energy-Efficient Variation-Resilient High-Throughput Processor Design," JECEI, 2021.
- J H. Dorosti, "Adaptive Energy-Efficient Variation-Aware Dynamic Frequency Management," JECEI, 2021.

PATENTS

- J IR Patent: 79179, Light Processor: Low-Power Processor for Wireless Sensor Networks, 16th April, 2013(1392/1/27).

COMPUTER SKILLS

- J Environments: Windows (9x, 2000, XP, Vista, 7 and 10), Linux.
- J Programming Languages: Java, C++/C/C#, and Visual Basic/Qbasic, Python, Perl, Bash scripting.
- J Hardware Description and Modeling Languages (HDLs): Verilog, VHDL, SystemC.
- J Software and design environments: MATLAB, MATLAB Toolboxes: [Signal processing, Filter design], Simulink, HSpice, Pspice, Modelsim, DXP, Proteus, CodeVision AVR, ATMEL Studio, Keil.
- J High performance computing and signal and image processing with CUDA and OpenCV.
- J VLSI CAD Tools: Sedit, Ledit, Leonardo, Simplicity, Quartus, ISE, Synopsis Design Compiler & Prime Power, Cadence SoC Encounter tools.
- J Web programming: PHP, HTML, Java script.
- J Simulators and profiling tools: SimpleScalar (both for MIPS and ARM), Sim-wattch, Opnet.
- J Parser generator tool: ANTLR.
- J Other utility softwares: Microsoft office (Word, Excel, Frontpage, Power point, Pubishier ...), Microsoft Visual Studio (2006, 2008 ...).

HONORS

-) Selected as “**First 10% top students**” by ECE to continue education in master degree without selection exam, Summer 2010.
-) Ranked **271th** among 250000 participants in nationwide university entrance exam, Summer 2005.

WORK EXPERIENCES

-) Design and implementation of GSM home appliances (air conditioning systems), Marsuscom co. (June, 2008 - March, 2011).
-) Design and implementation of Low-Power processor for Wireless Sensor Networks based on application classes, Silicon Intelligence and VLSI Signal Processing LAB, (June ,2010 – Dec., 2012)
-) Design and implementation of digital transponder (GEO stationary systems, Space applications), Moj-Pajuh co. (April, 2012 – April, 2014)
-) Design and implementation of inertial navigation system using gyro. MEMS sensor, ESP [co-operation].
-) Design and implementation of real-time high performance signal processing applications using CUDA platform, HR Co (May, 2014- April, 2018).
-) Design and implementation of AIS Base Station, Moj-Pajuh co [co-operation] (Jan., 2019-Sep., 2019).
-) Design and implementation of flight balance control system for quadcopters, ESP [co-operation].

ASIC DESIGN EXPERIENCES

-) Member of Light Processor (UTWP) Team, Design and Implementation of a low-power WSN processor, Silicon Intelligence and VLSI Signal Processing LAB, ECE Department, University of Tehran, 2011-2012.

TEACHING EXPERIENCES

-) Spring 2012: Assembly and Machine Language Programming, Shahid Rajae Teacher Training University.
-) Spring 2012: Computer Architecture Lab., Shahid Rajae Lecturer Training University.
-) Winter 2018: Hardware/Software Co-Design, Shahed University.
-) Winter 2018: Advanced Computer Architecture, Shahed University.
-) Spring 2018: Architecture of Object-Oriented Accelerators, Shahed University.
-) Spring 2018: Fault-Tolerant System Design, Shahed University.
-) Winter 2019: Hardware/Software Co-Design, Shahed University.
-) Winter 2019: Advanced Computer Architecture, Shahed University.
-) Winter 2019: DSP Processors, University of Eyvanekey.
-) Winter 2019: High-Performance Multi-Core Processors, University of Eyvanekey.
-) Spring 2019: Architecture of Object-Oriented Accelerators, Shahed University.
-) Spring 2019: Fault-Tolerant System Design, Shahed University.
-) Winter 2019: Discrete Mathematics, Shahid Rajae Teachre Training University.
-) Winter 2019: Data Structures, Shahid Rajae Teachre Training University.

PROFESSIONAL EXPERIENCE

- J Journal reviewer, Elsevier, Computers & Electrical Engineering (CEE), since 2012.
- J Conference reviewer, International Symposium on Computer Architecture & Digital Systems (CADS), 2013.
- J Journal reviewer, Journal of Electrical and Computer Engineering Innovations (JECEI), since 2019.
- J Journal reviewer, Journal of Circuits, Systems and Computers (JCSC), since 2016.

TEACHING ASSISTANT EXPERIENCES

- J Spring 2013: Custom Implementation of DSP Systems, Teaching assistant, School of Electrical and computer engineering, University of Tehran.
- J Spring 2013: Digital Electronics, Teaching assistant, School of Electrical and computer engineering, University of Tehran.
- J Fall 2012: Advanced VLSI, Teaching assistant, School of Electrical and Computer engineering, University of Tehran.
- J Fall 2012: VLSI System Design, Teaching assistant, School of Electrical and Computer engineering, University of Tehran.
- J Spring 2012: Custom Implementation of DSP Systems, Teaching assistant, School of Electrical and computer engineering, University of Tehran.
- J Spring 2012: Digital Electronics, Teaching assistant, School of Electrical and computer engineering, University of Tehran.
- J Spring 2011: Digital Electronics Lab, Supervisor, School of Electrical and computer engineering, University of Tehran.
- J Spring 2011: Custom Implementation of DSP Systems, Teaching assistant, School of Electrical and computer engineering, University of Tehran.
- J Spring 2011: Digital Electronics, Teaching assistant, School of Electrical and computer engineering, University of Tehran.
- J Fall 2010: Advanced VLSI, Teaching assistant, School of Electrical and Computer engineering, University of Tehran.
- J Fall 2010: VLSI System Design, Teaching assistant, School of Electrical and Computer engineering, University of Tehran.
- J Spring 2010: Digital Electronics, Teaching assistant, School of Electrical and computer engineering, University of Tehran.
- J Fall 2009: VLSI System Design, Teaching assistant, School of Electrical and Computer engineering, University of Tehran.
- J Spring 2009: Digital Electronics, Teaching assistant, School of Electrical and computer engineering, University of Tehran.
- J Spring 2009: Microprocessor Lab., Supervisor, School of Electrical and computer engineering, University of Tehran.
- J Spring 2009: Microprocessor, Teaching assistant, School of Electrical and Computer engineering, University of Tehran.
- J Fall 2008: VLSI System Design, Teaching assistant, School of Electrical and Computer engineering, University of Tehran.
- J Fall 2008: Microprocessor Lab., Supervisor, School of Electrical and Computer engineering, University of Tehran.

- J Fall 2008: Microprocessor, Teaching assistant, School of Electrical and Computer engineering, University of Tehran.
- J Summer 2008: Microprocessor Lab., Supervisor, School of Electrical and Computer engineering, University of Tehran.
- J Spring 2008: Microprocessor, Teaching assistant, School of Electrical and Computer engineering, University of Tehran.

SELECTED ACADEMIC PROJECTS

- J Winter 2012, Design and implementation of grid computing service composition using priority-based simulated annealing.
- J Winter 2011, Design and implementation of EMAIL content processing and spam detection algorithm in java.
- J Winter 2011, Design and implementation of NoC routing algorithm using Xmulator simulator in C#.
- J Winter 2011, Design and implementation of MRI image processing and Tumor detection in java.
- J Spring 2010, Design and implementation of a low power add-shift multiplier, using Modelsim and Synopsis design compiler and prime power tools, as final project of Low Power Integrated Circuits.
- J Spring 2010, Design and implementation of a digital filter in 3 methods, using MATLAB, Modelsim and Quartus, as final project of Custom implementation of Digital Signal Processors.
- J Fall 2009, Design and Implementation of FIR filter processor with VHDL.
- J Fall 2009, Provide a benchmark suit for network processors as final project of advanced computer architecture course.
- J Spring 2009, Design and Implementation of some I/O interface circuits such as USART, USB using Quartus as final project of Interface Circuit Design course.
- J Fall 2008, Design and Implementation of a Cheese game on Altera Cyclone FPGA using Quartus as project of Computer Architecture Lab.
- J Spring 2008, Design and Implementation of TCP over UDP in java as final project of Network course.
- J Spring 2008, Design and Implementation of a CPU on FPGA, using Quartus, as final project of Logic Lab.
- J Fall 2007, Design of an Operational Transconductance Amplifier (OTA), using HSPICE, as final project of Electronics II.
- J Fall 2007, Design and Implementation of a simple chat server with raw socket as project of Operating System course in C.
- J Fall 2007, Design and Implementation of a queue manager as project of Operating System course.
- J Fall 2007, Design and Implementation of a video game with ATMEL microcontrollers as final project of Microprocessor course.
- J Spring 2007, Design and implementation of Single Cycle, Multi Cycle and Pipeline processor using Modelsim as some projects of Computer Architecture course.
- J Spring 2007, Design and implementation of an IC language compiler in java as final project of Compiler Design course.
- J Fall 2005, Design and implementation of simple text editor (SMTE) as project of fundamentals of programming course in C.

LANGUAGE SKILLS AND QUALIFICATIONS

-) Native in Persian and Turkish, Fluent in English, Familiar with Arabic and French (to some extent).

HOBBIES

-) **Athletic:** Ping-Pong, Soccer, Kung fu, Wushu.
-) **Music:** Listening to Iranian traditional and pop music.
-) **Books:** reading science-fiction stories, philosophical books.